

1504/3061



**Europäisches
Patentamt**

**European
Patent Office**

**Office européen
des brevets**

1504/3061

MAILED 12 OCT 2004

WIPO

PCT

Bescheinigung

Certificate

Attestation

Die angehefteten Unterla-
gen stimmen mit der
ursprünglich eingereichten
Fassung der auf dem näch-
sten Blatt bezeichneten
europäischen Patentanmel-
dung überein.

The attached documents
are exact copies of the
European patent application
described on the following
page, as originally filed.

Les documents fixés à
cette attestation sont
conformes à la version
initialement déposée de
la demande de brevet
européen spécifiée à la
page suivante.

Patentanmeldung Nr. Patent application No. Demande de brevet n°

03300129.8

**PRIORITY
DOCUMENT**
SUBMITTED OR TRANSMITTED IN
COMPLIANCE WITH RULE 17.1(a) OR (b)

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

BEST AVAILABLE COPY



Anmeldung Nr:
Application no.: 03300129.8
Demande no:

Anmeldetag:
Date of filing: 23.09.03
Date de dépôt:

Anmelder/Applicant(s)/Demandeur(s):

Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
Si aucun titre n'est indiqué se referer à la description.)

High performance low noise amplifier

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s)
revendiquée(s)

Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/
Classification internationale des brevets:

H03F/

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of
filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL
PT RO SE SI SK TR LI

BEST AVAILABLE COPY

“High performance low noise amplifier.”

The invention concerns the field of radio receiver circuits. More particularly the invention relates to circuit topology of a signal processing circuit intended to be stacked with two quadrature mixer circuits. Such a signal processing circuit receives a pair of input signals in phase opposition on two input terminals and provide two pairs
5 of output currents in phase opposition on four output terminals, each input signals being amplified in an amplification unit and being split in a splitting unit. Said output terminals of said signal processing circuit are then connected to said mixer circuits in such a way that each mixer circuit receive a pair of signals that are in phase opposition. Such a pair of signals that are in phase opposition can also be called
10 differential signal, said differential signal meaning said pair of signals.

In its different applications, the invention notably relates to the reception of signals like, for example, radio signals, telecommunication signals, telephone signals, audio base-band signals, wireless analog signals, video signals etc...

The invention also concerns any receiver for such signals and chips intended
15 to be implemented in said receiver. Such receiver can be a phone in wireless standard, DECT for example, a radio receptor, a wireless controller...

First tasks realized in a reception chain RC as represented on Fig.1 in a radio receiver circuit are an amplification of signals in order not to corrupt said signals with
20 a too high noise floor and a frequency translation that allows further processing at a much lower signal frequency. As stated above, signals are, for example, radio frequency signals and are constituted of a pair of input signals that are in phase opposition S_p and S_n .

In such a reception chain, the use of two mixer circuits M_I and M_Q operated by
25 two local oscillation signals in quadrature, LOI and LOQ, allows an image rejection and consequently enhances the quality of the reception. Often, as with double-balanced Mixer from Gilbert, mixer circuits need currents at their inputs. It has to be noted that the term ‘mixer circuit’ designates here the part of the circuit that does the frequency translation, the signal processing circuit designating the part of the circuit
30 that prepares the input signal for entering into the mixer circuit. Thus, a Gilbert quad is a good example for a mixer circuit.

A single stage topology for a signal processing circuit as presented in the introduction is proposed in the European patent application EP0998025. As represented on Fig.2, I and Q transconductances are two duplicated amplification unit LNAU as used in the two-stage topology as described hereinbefore. Indeed, using four amplification transistors instead of two enables to use each amplification transistor as a transconductance. The two mixer circuits are directly connected on the collector of amplification transistors T_{Ip} , T_{Qp} , T_{In} , T_{Qn} in such a way that each mixer circuit receives a pair of signals in phase opposition. In this one-stage topology it is observed that local oscillation signals leak to radio signal inputs. This is especially a problem in architecture where frequencies of local oscillation signals and input signals are identical.

An advantage of one or more embodiments is thus to propose a circuit topology for a signal processing circuit offering improved performance in terms of linearity and noise performance. Moreover, the invention allows to reduce disturbances to the generation of local oscillation signals that are provided to mixer circuits.

To this end, the invention proposes that each of the two splitting units includes two branches connected between the respective amplification unit and one of the four output terminals, the four branches each including at least an impedance having identical characteristics.

This exemplary embodiment of the invention allows an improved noise performance since the input signal is not amplified to a large voltage at the frequency of the input signal. This topology allows better noise performance than the one-stage topology of the prior art. This presents a better isolation of the input signals from the local oscillation signals than with the one-stage topology of the prior art. Moreover, this may presents a good isolation of the generator of local oscillation signals to the disturbances that could be generated by input signals.

Alternatively, the impedance has a resistance value such that said value determines the splitting of the input signal independently of the stacked mixer circuits. Indeed, the split of current is determined by the matching of the splitting impedance rather than the matching from the transistors of the mixer circuits. It allows to keep these transistors small and thus fast, for an improved switching speed. This will turn into better noise performance.

An implementation of the amplification unit may use at least one amplification transistor of which base is connected to one input terminal and collector is connected to said splitting unit.

The invention also proposes embodiments that present a superior isolation of the input signals from disturbances generated by local oscillation signals.

Thus, in another exemplary embodiment, each of the four branches further includes a cascode transistor, bases of said four cascode transistors being connected together.

In an other embodiment, each of the two amplification units includes at least an amplification transistor of which base is connected to one input terminal and collector is connected to another transistor in cascode, said transistor in cascode being

BEST AVAILABLE COPY

connected by its collector to the respective splitting unit and being connected by its base to the transistor in cascode of the other amplification unit.

The invention also relates to a chip implementing a signal processing circuit according to the invention and a receiver including such a chip.

5

Additional objects, features and advantages of the invention will become apparent upon reading the following detailed description and upon reference to the accompanying drawings in which:

Fig.1 represents a schematic diagram of a reception chain as known in the prior art;

Fig.2 represents a signal processing circuit as known in the prior art;

Fig.3 represents a first embodiment for a signal processing circuit according to the invention;

Fig.4 represents a second embodiment for a signal processing circuit according to the invention;

Fig.5 represents a third embodiment for a signal processing circuit according to the invention;

Fig.6 represents a signal processing circuit according to the invention stacked with two mixers;

Fig.7 represents a block diagram of a receiver of radio frequency signals according to invention;

Fig.8 represents the local oscillation signals in the temporal dimension.

In the following description, well-known functions or constructions by the person skilled in the art are not described in detail since they would obscure the invention in unnecessary detail.

Fig.1 presents a schematic diagram of a reception chain RC as known in the prior art. This Figure is already described hereinabove. The invention concerns the topology of the signal processing circuit SPC. Consequently this schematic diagram also represents a reception chain RC as implemented in a chip according to the invention as soon as said signal processing circuit SPC is according to the invention.

Fig.2 presents a signal processing circuit as known in the prior art. Using this signal processing circuit, the same bias current is shared between said signal

processing circuit and mixer circuits. Effectively signals provided on outputs of four amplification transistors, of which bases are connected to the input signals, are currents. Said amplification transistors also constitute a splitting unit. This allows to directly connect a mixer circuit that requires a current input. The signal processing circuit SPC and mixer circuits are consequently stacked on each other. The advantage of a shared bias current with mixer circuits is also provided by the invention.

Fig.3 presents a first embodiment for a signal processing circuit SPC according to the invention. Said signal processing circuit is intended to receive a pair of input signals in phase opposition (S_n and S_p) on two input terminals and to provide two pairs of output currents in phase opposition (S_{In}, S_{Ip}) and (S_{Qn}, S_{Qp}) on four output terminals intended to be connected to said two mixer circuits. Each input signals S_n and S_p is amplified by a low noise amplification unit LNA_{Un} and LNA_{Up} and is split by a splitting unit SPL_{Un} and SPL_{Up} .

For example, said low noise amplification unit $LNAU$ is conventionally realized through an amplification transistor T_p and T_n . Signal S_n is provided to the base of an amplification transistor T_n and signal S_p is provided to the base of an amplification transistor T_p . Said amplification transistors T_p and T_n are biased by a common biasing intensity I_{bias} , connected through an inductive element L_p and L_n to the emitter of said amplification transistors T_p and T_n . Collector of each amplification transistor T_p and T_n is connected to the respective splitting unit SPL_{Up} and SPL_{Un} .

A splitting unit $SPLU$ includes two branches called BI and BQ . In this paragraph, only the splitting unit SPL_{Up} for the signal S_p is described. The description would be similar for the signal S_n by replacing p by n in the references. The two branches BI_p and BQ_p are connected at a node E_p connected to said amplification unit LNA_{Up} and one of said output terminals. Each branch BI_p and BQ_p respectively includes at least an identical low value resistance R_{Ip} and R_{Qp} . The role of such resistors R_{Ip} and R_{Qp} is that the accuracy of the current splitting is realized through said resistor instead of the transistors of the mixer circuits. Typically the DC voltage to be applied to the splitting unit is $2 \cdot V_T = 50mV$ in order to get rid of the influence of the resistance of the mixer circuits and their loads, constituted by Gilbert quads for example. The matching is thus made by the resistors of the splitting unit independently of the resistance of the mixer circuits and their load. The DC voltage at the terminals of a load resistor is generally around $800mV$. The resistor of the splitting

unit is thus advantageously $800/50=16$ times smaller than a load resistor. The current arriving on node Ep is thus split between the two branches thanks to the presence of the two resistances of the splitting unit. As these resistances are of a low value, they do not introduce any gain. Moreover large voltage headroom is available as only one transistor is used and resistances are of low value.

Fig.4 presents another exemplary embodiment for a signal processing circuit according to the invention. The embodiment of Fig.4 proposes to add another transistor in cascode TCp and TCn in each amplification unit LNAUp and LNAUn. Such a transistor in cascode TCp and TCn has an isolation function against the leaks from local oscillation signals LO to the input signal S. For the p side, said transistor in cascode TCp is connected, by its emitter to the amplification transistor Tp and by its collector to said splitting unit SPLUp and by its base to the transistor in cascode-TCn of the other amplification unit LNAUn. The voltage headroom is reduced but the disturbance caused by local oscillation to the input signal is reduced.

Fig.5 presents yet another embodiment for a signal processing circuit. In this embodiment, the above-presented isolation is realized through cascode transistors inserted on each branch of the two splitting unit SPLUp and SPLUn. Bases of the four cascode transistors are connected together. This solution may be useful for architectures where the disturbances from local oscillation signals to input signals are important.

The main parameters to be adjusted for a reception chain as generically presented on Fig.1 are the noise, the linearity, the local oscillation disturbances, the dissipated power and the die area. These parameters are more or less critical depending on the application to which the reception chain is dedicated.

The noise is mainly created by transistors of the circuit. The main noise contributors are shot noise and thermal noise of input transistors, base and collector. This noise is identical for any implementations of the transistor. Equivalent input voltage and current noise contributors are identical.

Linearity properties are similar and better for all presented one-stage topologies than for the two-stage topology.

The local oscillation disturbances are critical. Especially the application where the local oscillation signals might be disturbed by the input radio signals (ZIF applications...) This is related to the so-called local oscillation pulling phenomenon :

oscillators are very sensitive to disturbances that arise close to their oscillation frequency. Thus in the ZIF architecture, the oscillator frequency is equal to the RF frequency, or one of its harmonics.

5 The dissipated power is usually a significant portion of overall circuit consumption.

The die area is generally not very critical for this kind of circuit.

As represented on Fig.6, a very popular circuit for the mixer circuit is the double-balanced Mixer from Gilbert, called Gilbert quad. A Gilbert quad translates signals S at input frequency INF to signals IS at intermediate frequency IF. The
10 intermediate frequency IF depends upon the local oscillation signal frequency LOF as $IF = INF - LOF$.

It is important to note that the output from the Gilbert quad is a current, rather than a voltage. For this reason, a current to voltage load MLD_I, MLD_Q, e.g. a simple resistor RIp, RIn, RQp, RQn, needs to be connected at the mixer outputs on
15 which output signals ISIp, ISIn, ISQp and ISQn are provided. Capacitors CI and CQ are implemented to filter out out-of-channel interferences that can exist when running at intermediate frequency IF.

Moreover the signal processed by a Gilbert quad is also a current. This is the reason why the signal fed from the signal processing circuit SPC to the mixer circuit is
20 a current.

Consequently a signal processing circuit providing a current at its outputs can directly be stacked with mixer circuits. Thus, Fig.6 presents a signal processing circuit according to the invention stacked with two mixers. Such stacked circuits are thus reproduced on a chip according to the invention. Said chip generally includes other
25 functions for the functioning of a receiver of the invention as represented in Fig.7.

The properties of the different signal processing circuit embodiments of the invention and of the prior art will now be described and compared.

The signal processing circuit represented on Fig.2 has noise and linearity properties superior to the ones of a two-stage topology, especially at large emitter
30 degeneration. Nevertheless it presents drawbacks as above stated.

The signal processing circuit represented on Fig.3 presents very good overall performance. It offers a large voltage headroom. The current split is determined by the mixers that are connected on outputs of said signal processing circuit and by the

resistors R_{Ip} , R_{In} and R_{Qp} , R_{Qn} . The splitting of the current is based on the differential local oscillation signals having identical swings and common mode. In the temporal dimension as represented on Fig.8, the two below presented cases are possible.

5 If $LO_{Ip}=LO_{Qp}$ and are superior to $LO_{In}=LO_{Qn}$ (point at time $T1$ on Fig.8), the current delivered by T_p is equally divided between R_{Ip} and R_{Qp} as expected. This is similar for T_n and the n side. All other combinations with local oscillation signals in opposite states give a similar half-half split.

10 If LO_{Ip} is greater than $LO_{Qp}=LO_{Qn}$ that's LO_{Ip} greater than LO_{In} (point at time $T2$), that means that LO_I is in one state and that LO_Q is changing from one state to the other. This is the case as the four signals LO_{Ip} , LO_{In} , LO_{Qp} , LO_{Qn} all have the same continuous-part-DC, but different phases. Transistor's emitters follow the one that has the higher potential. Thus, the current delivered by T_p is flowing totally into R_{Ip} and then to the mixer circuit M_I . Consequently the burst of noise coming from
15 the mixer M_Q , when at equilibrium, is very low since the mixer M_Q is off. This advantage is not present in the state of the art as transistors in mixer circuits never behave as diodes during operation because of a transistor's emitter effect. In other topologies of the state of the art, the I side has no influence on the Q side. This is different in the invention because of the structure of the splitting unit. Because of the
20 presence of a resistance in the splitting unit, the sum of the p and n signals presents variations because of the transistor's emitter effect. Another advantage is that no current is lost in the mixer with temporary no gain (M_Q here). It makes overall mixer gain higher. This is similar for T_n and the n side.

25 The I - Q gain matching, in order to have the same gain on each I and Q side, is determined by the matching of the resistors R_I and R_Q and, in a smaller extent, of the transistors of the I and Q mixer circuits.

On Fig.4, cascode transistors TC_p , TC_n are inserted in the amplification units. Their role is to absorb the disturbances generated from local oscillation signals to input signals. Consequently the signal processing circuit as presented on Fig.4
30 presents a better isolation of input signals.

On Fig.5, cascode transistors TC_{Ip} , TC_{Qp} , TC_{In} , TC_{Qn} are inserted in the splitting unit above the resistors. Their role is also to absorb the disturbances generated from local oscillation signals to input signals. In this embodiment, if resistors R_{In} ,

RIp, RQp, RQn are omitted (that is set to zero value) then the gain matching depends on the cascode transistors matching, which calls for big cascode transistors. On the other hand, a non zero resistor value, as on Fig.3, can introduce the Miller effect. A compromise can be realized by the man skilled in the art between the cascode transistor size and the value of the resistor.

Gain for the signal processing circuits presented on Fig.2 to Fig.5 is:

$$G = gm \cdot \frac{1}{2} \cdot \frac{2}{\pi} \cdot R = \frac{2}{\pi} \cdot \frac{V_R}{VT} = \frac{2}{\pi} \cdot \frac{0.8}{0.025} = -4 + 30 = 26dB$$

This calculation is done assuming that the amplification transistor emitter degeneration does not change very significantly the gain (in practice it might be some -3 dB), that the size of amplification transistors of the signal processing circuit of Fig.2 are half of amplification transistors of the embodiments of the invention. Current density is therefore identical for all presented circuit topologies. Consequently, overall base resistors of amplification transistors are equal for all topologies. Moreover the mixer gain is assumed ideal and equals -4dB (2/pi).

Conventions are:

gm is the amplification unit input transconductance,
R is the mixer load.

This gain is slightly inferior to the one obtained with the two-stage topology that is around 30 dB.

At low emitter degeneration, the main noise contributors of all topologies, including the one of the prior art, are identical. One-stage topologies have fewer components to contribute to noise. It is balanced by the mixer circuits that are slightly noisiest because there was a bit less gain in front of it. On embodiments presented on Fig.3 and 4 a noise term depending on commutation speed of the quad is fairly reduced. Voltage headroom is more comfortable with only two stacked transistors, consequently for the embodiment presented on Fig.3.

The isolation of the input signal from the local isolation leaks is very good for the embodiments presented on Fig.4 and 5.

The isolation of the local oscillation signals from the input signals leaks is weak in two-stage topologies where the input voltage is amplified. The embodiment presented on Fig.5 amplifies the input signal on top of the amplification transistors and

as the current split is done with resistors, leaks can occur. The other embodiments of the invention present a good isolation.

Benefits of the one or more embodiments of the invention are superior noise performance at lower bias current. Embodiments that present a reduced impact on pulling of the input signal to the local oscillation signals are also proposed.

An application of the invention concerns reception chains as small signals have to be processed. Nevertheless, a circuit as described in Fig.6 can also be used in a transmission chain for example to have good linearity characteristics. As larger signals are processed, the use of the invention is less critical but can be advantageous.

Fig.7 presents a block diagram of a receiver of radio frequency signals according to the invention. Generally such a receiver is intended to receive and to transmit signals through an antenna ANT. A commutation device COM controls the access to the antenna ANT. Said commutation device COM is connected at least to a reception chain RX and to a transmission chain TX. Said reception chain RX includes at least a signal processing circuit SPC according to the invention and a frequency translation unit FTCT, generally constituted of mixer circuits. A processing unit MC follows these circuits. This processing unit MC also processes the signals to be transmitted and is thus connected to a transmission chain TX that includes at least a frequency translation unit FTCT and an amplification unit AMPT. Such a receiver is advantageously a telecommunication apparatus: mobile phone...

The embodiment as disclosed on Fig.3 and the embodiments presented in Fig.4 and 5 are not exclusive. Other alternative embodiments may be derived in accordance with principles of the invention defined in the Claims to accomplish the same objectives.

It is to be understood that the present invention is not limited to the aforementioned embodiments and variations and modifications may be made without departing from the spirit and scope of the invention as defined in the appended claims. In the respect, the following closing remarks are made.

It is to be understood that the present invention is not limited to the used transistors type. Similar embodiments can use other type of transistor types, e.g. MOS... Resistive emitter degeneration can be used rather than inductive. However, inductive degeneration allows superior noise performance. Also, a current source, often implemented as a pure resistance connected from the power supply to the

emitters of the cascode transistors, or to the emitters of the Gilbert quads can be added. It allows to get both a high input transconductance from the input pair, and a low voltage drop across the resistor load.

5 It is to be understood that the invention is not limited to the aforementioned telecommunication application. The invention can be used within any application using a reception chain needing a frequency translation before further processing. Radio frequency application are thus very concerned by the invention.

10 Any reference sign in the following claims should not be construed as limiting the claim. It will be obvious that the use of the verb "to comprise" and its conjugations do not exclude the presence of any other steps or elements besides those defined in any claim. The article "a" or "an" preceding an element or step does not exclude the presence of a plurality of such elements or steps.

Claims:

1. A signal processing circuit intended to be stacked with two mixer circuits, said signal processing circuit being intended to receive a pair of input signals in phase opposition on two input terminals and to provide two pairs of output currents in phase opposition on four output terminals intended to be connected to said two mixer circuits in order that each mixer circuit receives one pair of output currents in phase opposition, each input signals being amplified by a respective low noise amplification unit and being split by a respective splitting unit, characterized in that each of the two splitting units includes two branches connected between the respective amplification unit and one of the four output terminals, the four branches each including at least an impedance having identical characteristics.
2. A signal processing as claimed in Claim 1, wherein the impedance has a resistance value such that said value determines the splitting of the input signal independently of the stacked mixer circuits.
3. A signal processing circuit as claimed in one of the claims 1 and 2, wherein each four branches further includes a cascode transistor, bases of said four cascode transistors being connected together.
4. A signal processing circuit as claimed in one of the Claims 1 to 3, wherein each of the two amplification units includes at least one amplification transistor of which base is connected to one input terminal and collector is connected to respective splitting unit.
5. A signal processing circuit as claimed in one of the claims 1 and 2, wherein each of the two amplification units includes at least an amplification transistor of which base is connected to one input terminal and collector is connected to another transistor in cascode, said transistor in cascode being connected by its collector to respective splitting unit and being connected by its base to the transistor in cascode of the other amplification unit.

- 5 6. A chip intended to be implemented in a receiver, said chip including at least a signal processing circuit and two mixer circuits receiving local oscillation signals in phase quadrature, said output terminals of said signal processing circuit being connected to said mixer circuits in such a way that each mixer circuit receive a pair of signals that are in phase opposition, characterized in that said signal processing circuit is as claimed in one of claims 1 to 5.
- 10 7. A receiver of radio-frequency signals including at least an antenna, a reception chain, a processing unit, characterized by it includes a chip as claimed in claim 6.
-

“High performance low noise amplifier.”

Abstract:

A signal processing circuit is proposed where said circuit is intended to receive a pair of input signals S_p and S_n in phase opposition on two input terminals and to provide two pairs of output currents S_{Ip} and S_{In} in phase opposition on four output terminals. Each input signal S_p and S_n is amplified in an amplification unit LNAUp and LNAUn and subsequently split in a splitting unit SPLUp and SPLUn. The invention is such that each of the two splitting units SPLUp and SPLUn includes at least two branches, respectively BIp, BQp and BIn, BQn connected between said amplification unit, respectively LNAUp and LNAUn and one of said output terminals, the four branches BIp, BQp and BIn and BQn each including at least an impedance, respectively RIp, RQp, RIn, RQn having identical characteristics.

Mixer circuits can be easily stacked with this signal processing circuit.

Application: Radio-frequency reception chain

FIG.3

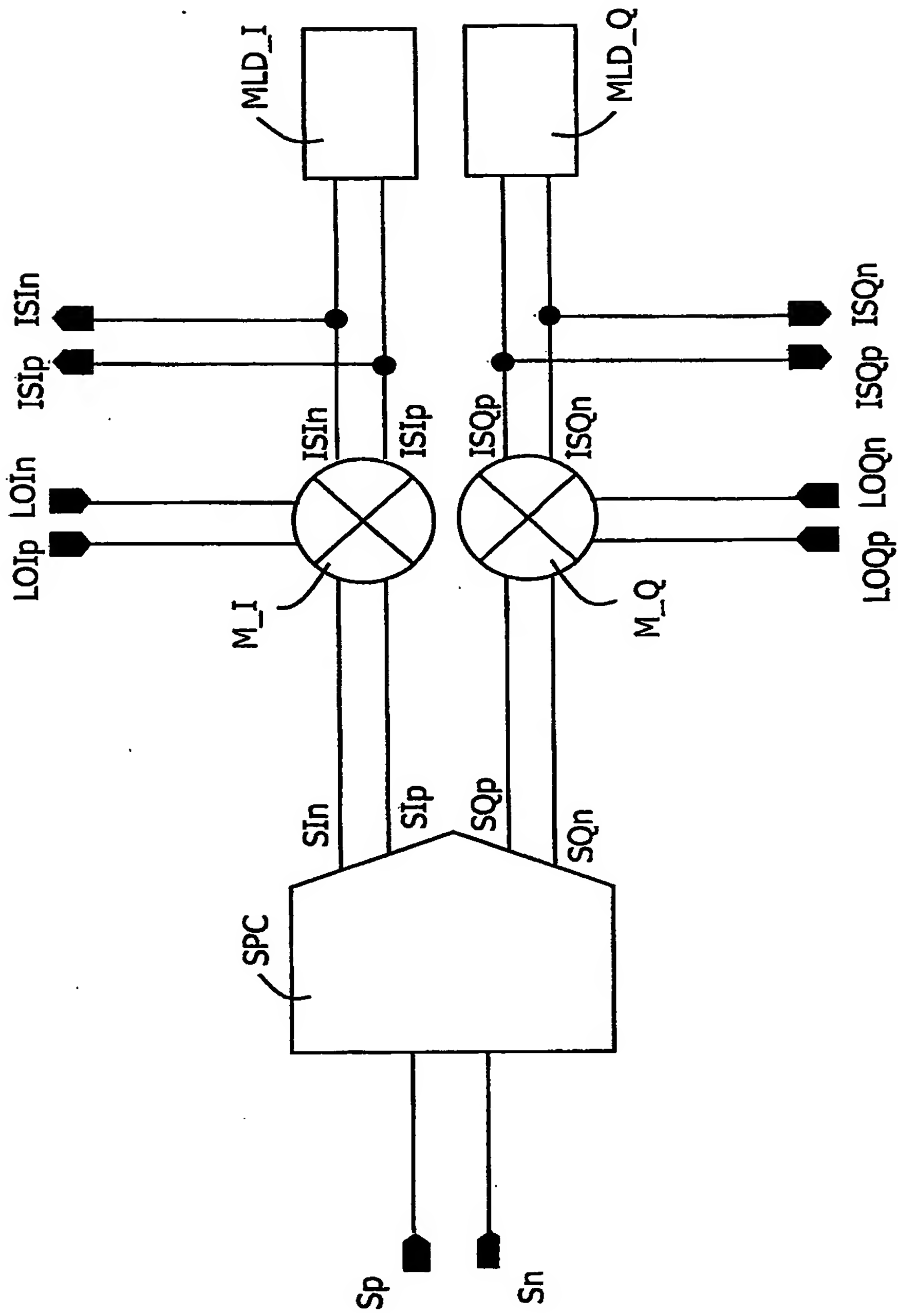


FIG. 1

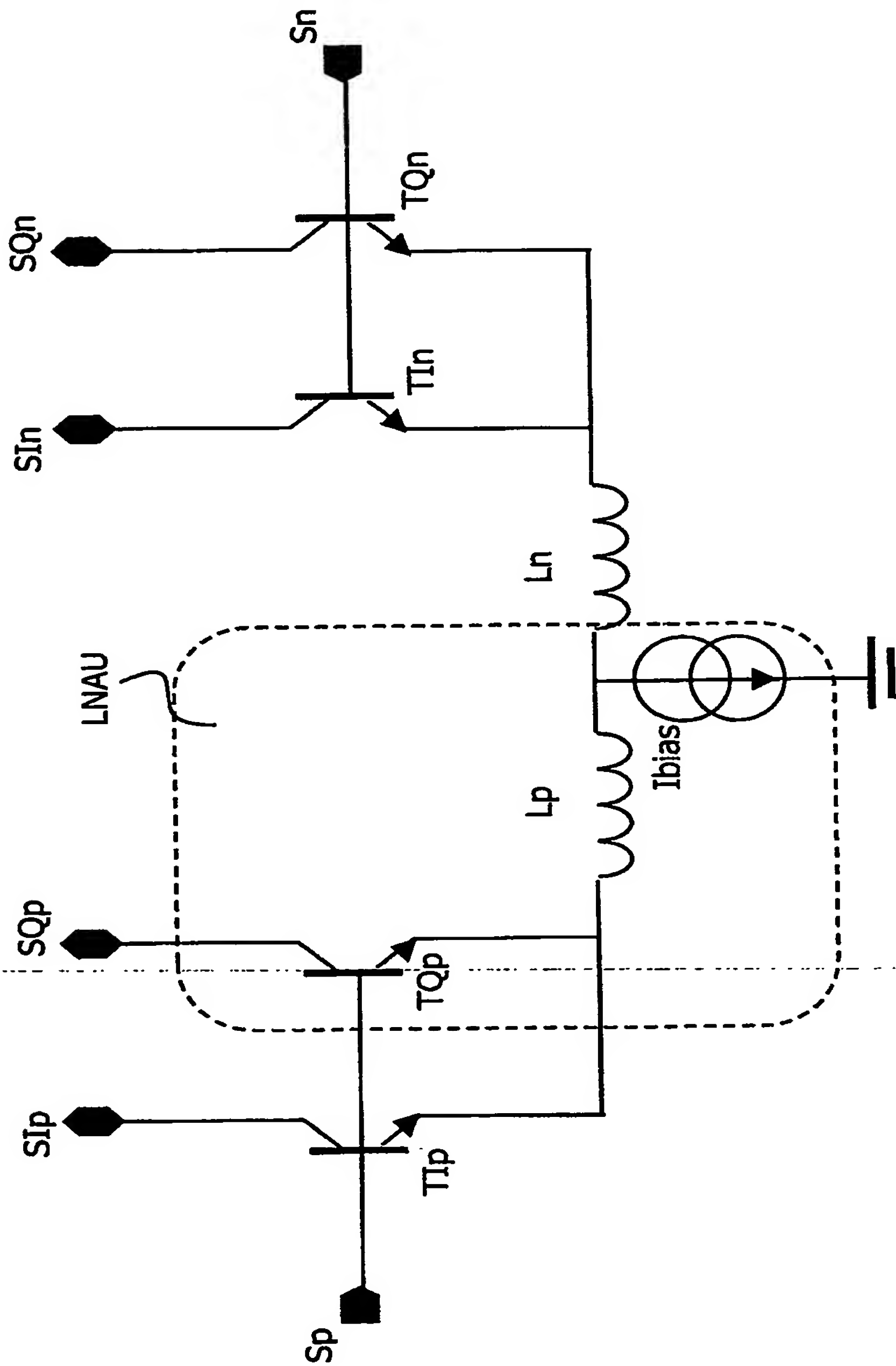


FIG. 2

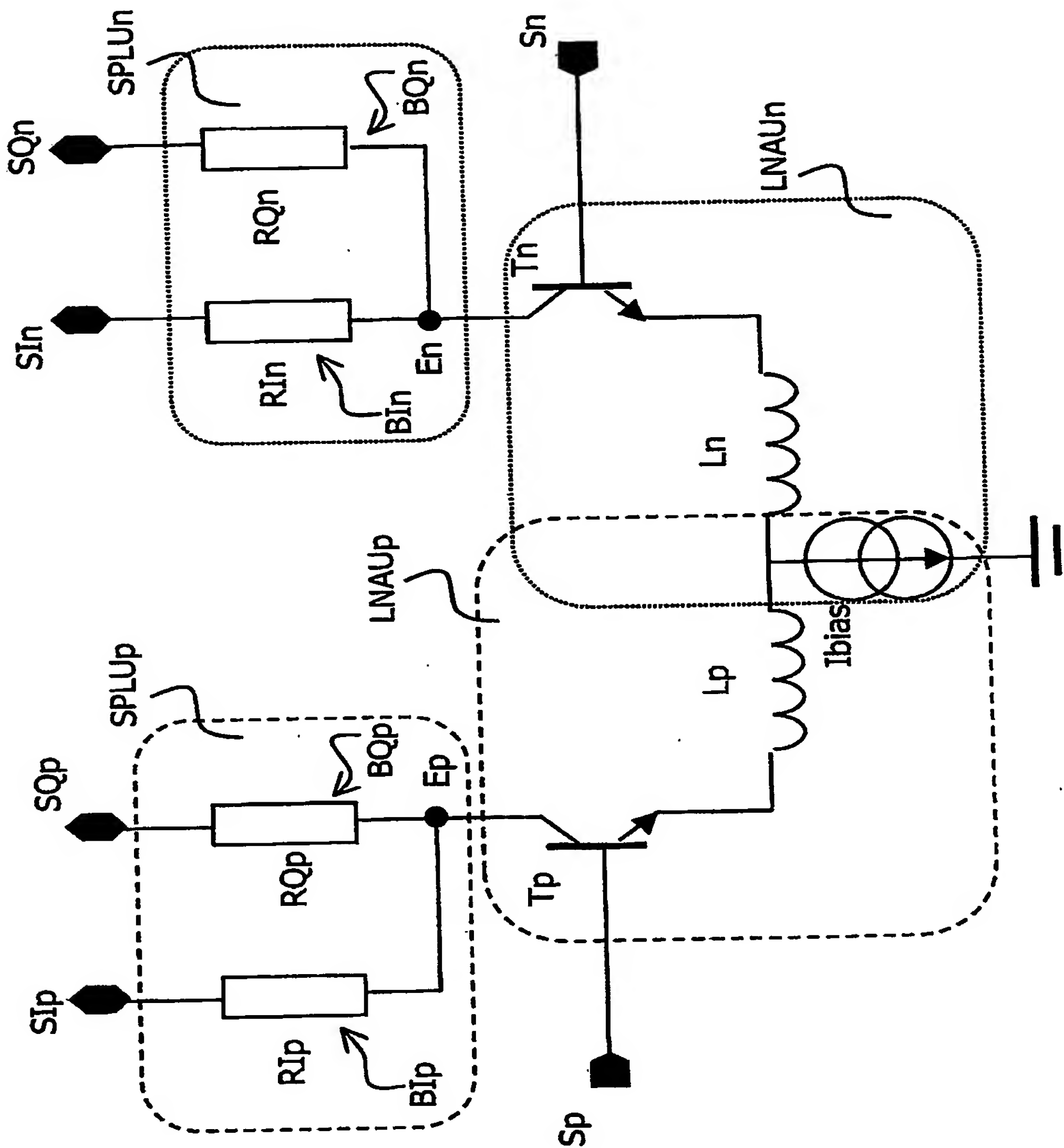


FIG. 3

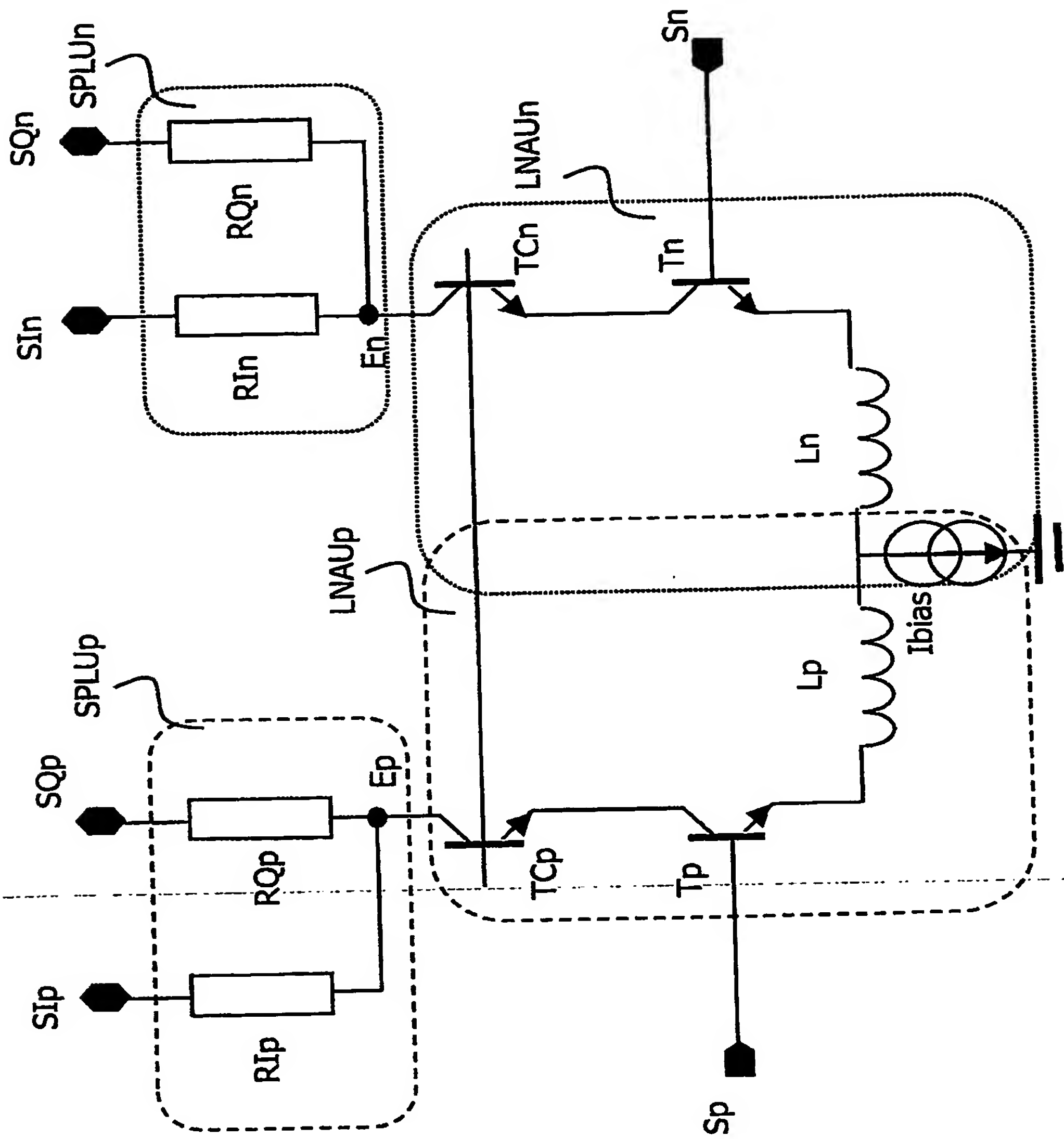


FIG. 4

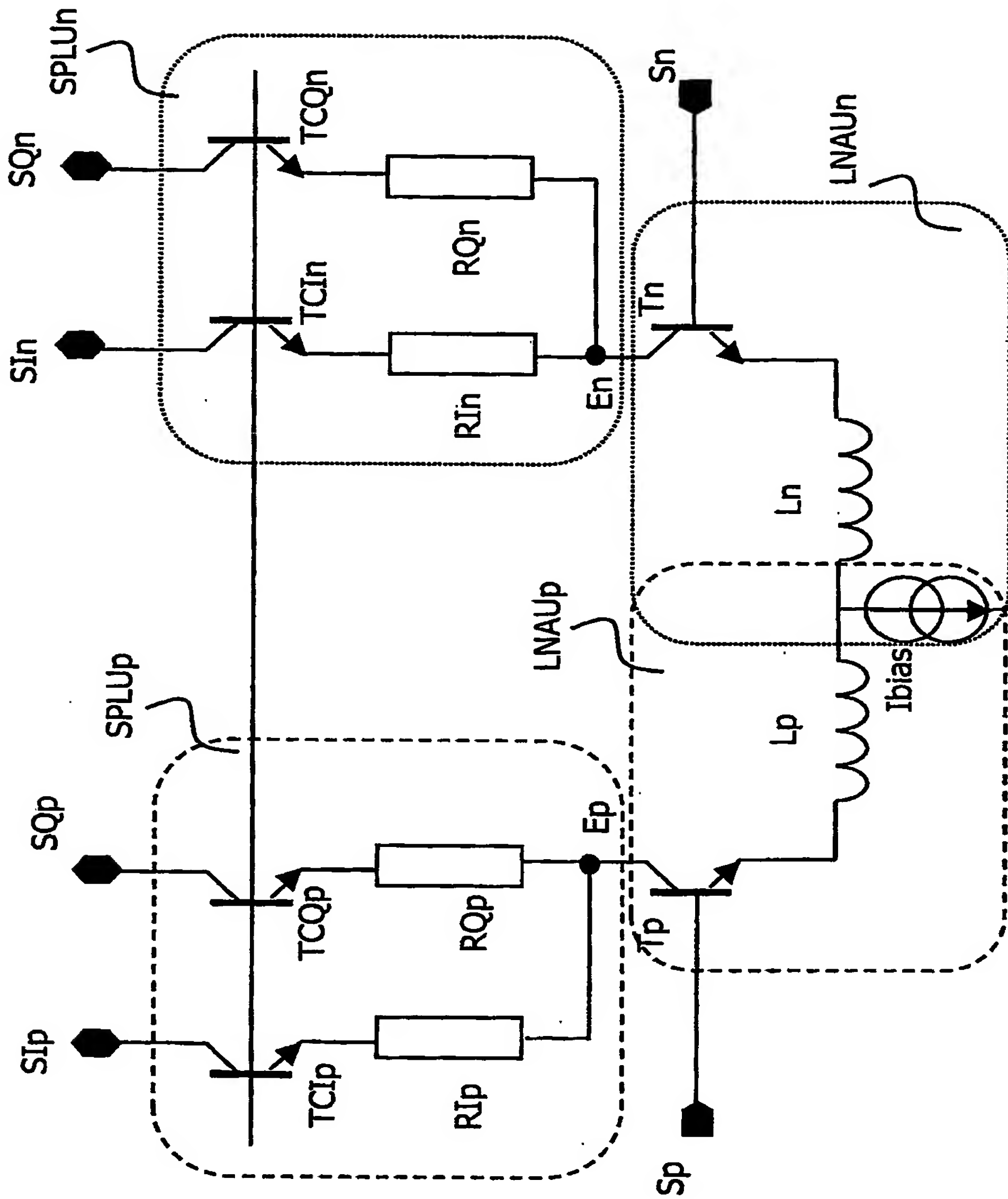


FIG. 5

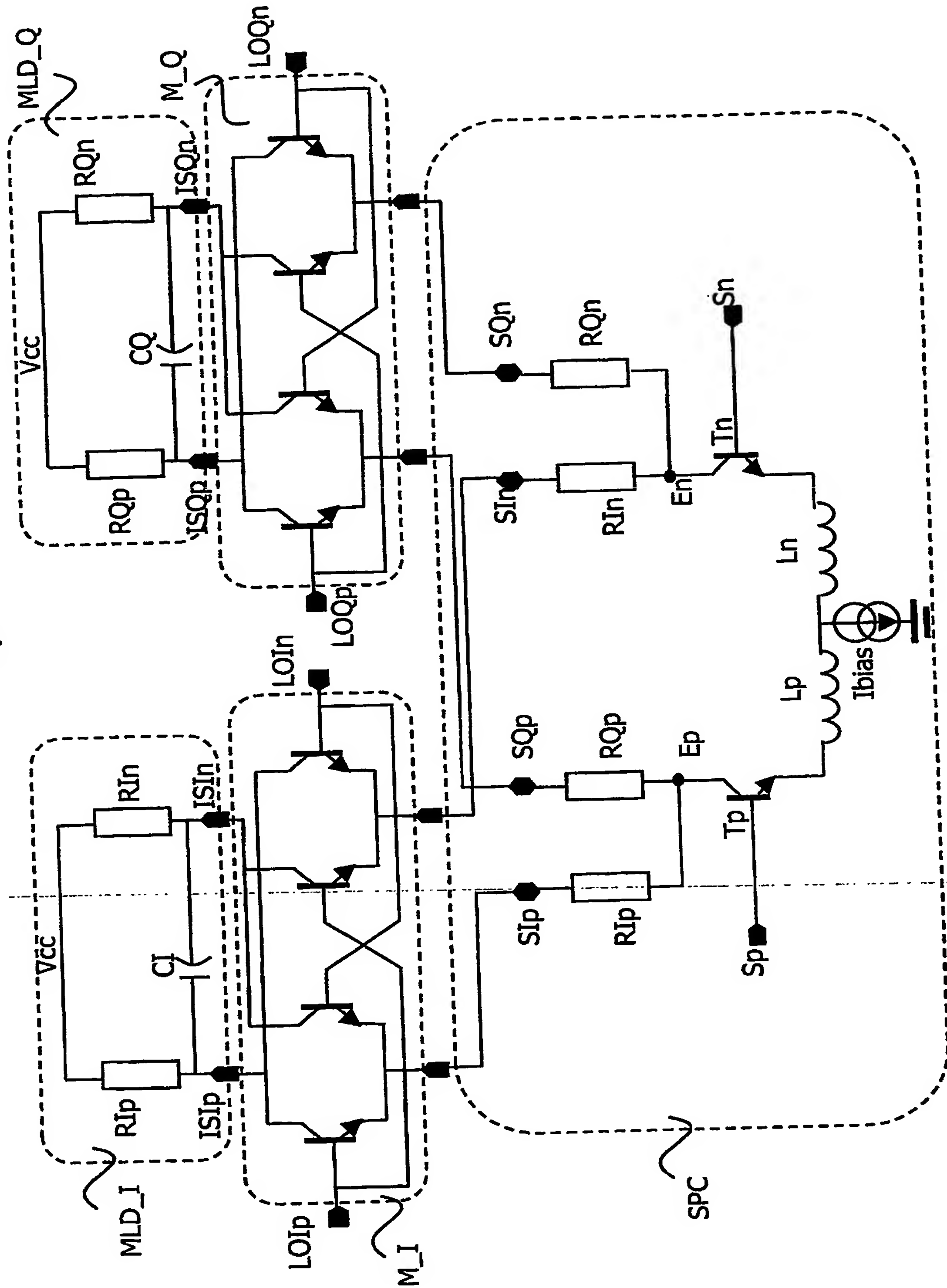


FIG. 6

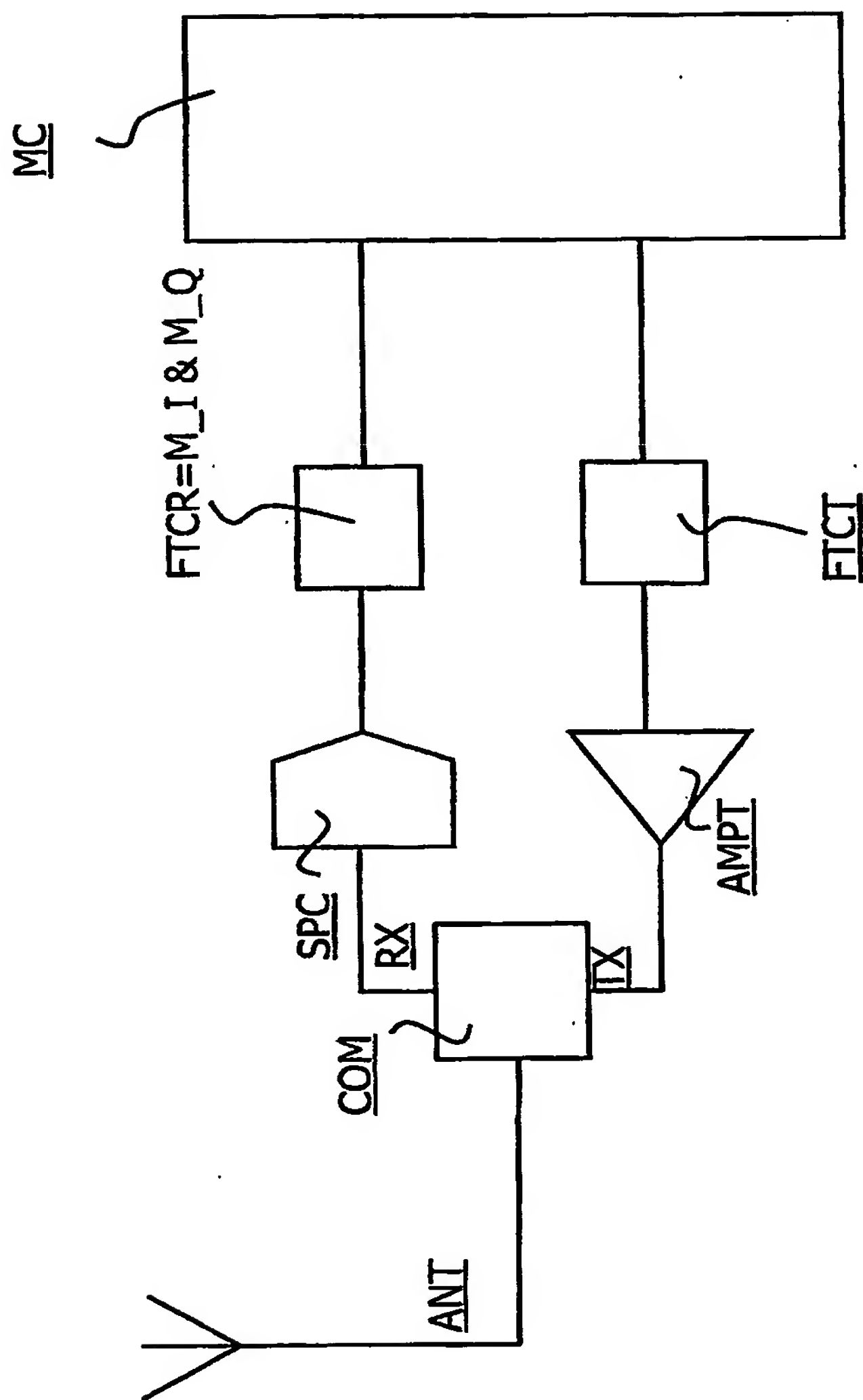


FIG. 7

